IN THE CLAIMS:

Please cancel claim 3 without prejudice or disclaimer. Please amend the remaining claims as follows:

1. (Currently Amended) A method for evaluating gate timing in an integrated circuit (IC) design, said method comprising:

determining when a first-type of signal is present on an input to a logical gating device, wherein said first-type of input signal allows transitions on an output of said logical gating device;

determining when a second-type of signal is present on said input, wherein said second-type of input signal inhibits transitions on said output of said logical gating device; and

modifying a timing of a sensing of said first-type of signal to sense said first-type of signal at an earlier point in time than said second-type of signal is sensed.

2. (Currently Amended) The method of claim 1, wherein:

said input comprises a gate input;

said first-type of signal and said second-type of signal comprise gating signals; and

said first-type of signal and said second-type of signal control whether pulses on a clock input of said logical gating device are propagated to said output of said logical gating [gate] device.

3. (Canceled).

4. (Currently Amended) The method of claim [2] 1, wherein said first-type of signal allows [said] clock pulses to be propagated on said output of said logical gating device and said second-type of signal prevents said clock pulses from being propagated on said output of said logical gating device.

5. (Currently Amended) The method of claim [2] 1, wherein said sensing [time] is used in computing a setup test.

6. (Currently Amended) The method of claim [3] 1, wherein said sensing [time] is used in computing a hold test.

7. (Currently Amended) The method in claim [2] 1, wherein said modifying prevents a delay in propagation of [said] gating signals across said logical gating device from inappropriately outputting a portion of a clock pulse.

8. (Currently Amended) The method of claim 1, wherein said modifying [includes] is performed assuming there is no load on said output.

9. (Currently Amended) The method in claim 1, wherein said modifying includes identifying a beginning point of a transition of said first-type of signal as [said sensing time] a time when said first-type signal is sensed.

10. (Currently Amended) The method of claim [4] 5, wherein the computing of said setup test comprises:

computing a propagated mode test value,

computing an input-to-input test value of zero, and

using the less pessimistic of said computed test values.

11. (Currently Amended) A method for evaluating gate timing in an integrated circuit (IC) design, said method comprising:

determining when a first-type of signal is present on an input to a logical gating device, wherein said first-type of input signal allows a clock pulse to be output from said logical gating device;

determining when a second-type of signal is present on said input, wherein said second-type of input signal inhibits said clock pulse from being output from said logical gating device; and

modifying a timing of a sensing of said first-type of signal to sense said first-type of signal at an earlier point in time than said second-type of signal is sensed.

12. (Original) The method of claim 11, wherein:

said input comprises a gate input;

said first-type of signal and said second-type of signal comprise gating signals.

13. (Currently Amended) The method of claim 11, further comprising performing a hold test between said input and a clock input of said logical gating device.

14. (Currently Amended) The method in claim 11, wherein said modifying prevents a delay in propagation of [said] gating signals across said logical gating device from inappropriately outputting a portion of said clock pulse.

15. (Currently Amended) The method of claim 11, wherein said modifying [includes] is performed assuming there is no load on said output.

16. (Currently Amended) The method in claim 11, wherein said modifying includes identifying a beginning point of a transition of [said input toward] said first-type of signal as [said sensing time of said first-type of signal] a time when said first-type signal is sensed.

17. (Currently Amended) A program storage device readable by machine, tangibly embodying a program of instructions executable by said machine for performing a method of evaluating gate timing in an integrated circuit (IC) design, said method comprising:

determining when a first-type of signal is present on an input to a logical gating device, wherein said first-type of input signal allows transitions on an output of said logical gating device;

determining when a second-type of signal is present on said input, wherein said second-type of input signal inhibits transitions on said output of said logical gating device; and

modifying a timing of a sensing of said first-type of signal to sense said first-type of signal at an earlier point in time than said second-type of signal is sensed.

18. (Original) The program storage device of claim 17, wherein:

said input comprises a gate input;

said first-type of signal and said second-type of signal comprise gating signals; and

said first-type of signal and said second-type of signal control whether pulses on a clock input of said logical gating device are propagated to said output of said gate device.

19. (Currently Amended) The program storage device of claim [18] 17, wherein said first-type of signal allows [said] clock pulses to be propagated on said output of said logical gating device and said second-type of signal prevents said clock pulses from being propagated on said output of said logical gating device.

20. (Currently Amended) The program storage device of claim 18, further comprising performing a hold test between said input and said clock input of said logical gating device.

21. (Currently Amended) The program storage device in claim [18] 17, wherein said modifying prevents a delay in propagation of [said] gating signals across said logical gating device from inappropriately outputting a portion of a clock pulse.

22. (Currently Amended) The program storage device of claim 17, wherein said modifying [includes] is performed assuming there is no load on said output.

23. (Currently Amended) The program storage device in claim 17, wherein said modifying includes identifying a beginning point of a transition of [said input toward] said first-type of

signal as [said sensing time of said first-type of signal] a time when said first-type signal is sensed.

Please add the following new claims:

24. (Newly Added) A method for evaluating gate timing in an integrated circuit (IC) design, said method comprising:

determining when a rising gating signal is present on an input to a logical gating device, wherein, after rising, said gating signal allows transitions on an output of said logical gating device; and

modifying a timing of a sensing of said rising gating signal to sense said rising gating signal at a point in time earlier than a midpoint between a low gating signal and a high gating signal.

25. (Newly Added) The method of claim 24, wherein said gating signal controls whether pulses on a clock input of said logical gating device are propagated to said output of said logical gating device.

26. (Newly Added) The method of claim 24, wherein said sensing is used in computing one of a setup test and a hold test.

27. (Newly Added) The method of claim 24, wherein said modifying prevents a delay in propagation of gating signals across said logical gating device from inappropriately outputting a portion of a clock pulse.

28. (Newly Added) The method of claim 24, wherein said modifying is performed assuming there is no load on said output.

29. (Newly Added) The method of claim 24, wherein said modifying includes identifying a beginning point of a transition of said gating signal as a time when said gating signal is sensed.

30. (Newly Added) A method for evaluating gate timing in an integrated circuit (IC) design, said method comprising:

determining when a rising gating signal is present on an input to a logical gating device, wherein, after rising, said gating signal allows transitions on an output of said logical gating device; and

modifying a timing of a sensing of said rising gating signal to sense said rising gating signal at a point in time earlier than a midpoint between a low gating signal and a high gating signal by reducing slew by a predetermined constant.

31. (Newly Added) The method of claim 30, wherein said gating signal controls whether pulses on a clock input of said logical gating device are propagated to said output of said logical gating device.

32. (Newly Added) The method of claim 30, wherein said sensing is used in computing one of a setup test and a hold test.

33. (Newly Added) The method of claim 30, wherein said modifying prevents a delay in propagation of gating signals across said logical gating device from inappropriately outputting a portion of a clock pulse.

34. (Newly Added) The method of claim 30, wherein said modifying is performed assuming there is no load on said output.

35. (Newly Added) The method of claim 30, wherein said modifying includes identifying a beginning point of a transition of said gating signal as a time when said gating signal is sensed.